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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/867,893	05/30/2001	Peter Thueringer	AT 00034	7109

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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BRIARCLIFF MANOR, NY 10510

EXAMINER	
PATEL, NITIN C	
ART UNIT	**PAPER NUMBER**
2116	

DATE MAILED: 10/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/867,893	THUERINGER ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in responsive to amendments filed on September 8, 2004.

2. Claims 6 – 13 have been added new.

3. Claims 1 –13 are pending with the application.

Claim Objections

4. Claim 10 is objected to because of the following informalities:

5. In the claim 10, in line7 "reducing the internal power source" should be "reducing the voltage on the internal power source".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 6 – 13 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Shamir, US Patent 6,507,913.

8. As to claim 6, Shamir teaches a device [10, smart card] comprising:

a. a processor [12, smart card chip] that is configured to process data [it is inherent to the smart card chip],

b. a capacitor [11] that is configured to provide power to the processor [12], and

c. a controller [15, switchover logic and 14 two power transistors] that is configured to: decouple [disconnect] the capacitor [11] from a power source [13, external power] at a first time, monitor a voltage on a capacitor [monitoring a voltage is inherently taught as switchover logic trigger by the threshold voltage] and interrupt the processor [event based interrupting is inherent to the processor] at a second time after the first time if the voltage on the capacitor falls to a first voltage level, discharge the capacitor at a third time after the first time, and couple the capacitor to the power source at a fourth time after the third time, so that power consumed by the processor between the first and third times is substantially masked [detachment]from power provided by the power source [during security critical computations], and wherein the third time is dependent upon an interval between the second and third times of a prior sequence of interrupting the processor and discharging the capacitor [switchover logic is triggered by a voltage of the discharging capacitor falling below predetermined threshold or by counting number of instructions which inherently measures time interval, or by combination of these factors][col. 3, lines 11 – 48, col. 4, lines 1 – 47, lines 58 – 67, col. 5, lines 1 – 40, fig. 2].

9. As to claim 10, Shamir discloses a method of masking [isolating] power consumption of a processor [from power supply] comprising:

a. decoupling [disconnecting] an internal power source [3, 4, capacitors] from an external power source [2] at a first time,

b. monitoring a voltage on the internal power source [monitoring a voltage is inherently taught as switchover logic trigger by the threshold voltage] and interrupting the processor [event based interrupting is inherent to the processor] at a second time after the first time if the voltage on the internal power source [capacitor voltage] falls to a first voltage level,

c. reducing the voltage on the internal power source [capacitor voltage] at a third time after the first time, and

d. coupling the internal power source [capacitor] to the external power source [2] at a fourth time after the third time, so that power consumed by the processor between the first and third times is substantially masked from power provided by the external power source, and,

e. modifying [alternatively] the third time for a subsequent repetition [charging and discharging of capacitors in periodic way] of the method, based on an interval between the second time and the third time [switchover logic is triggered by a voltage of the discharging capacitor falling below predetermined threshold or by counting number of instructions which inherently measures time interval, or by combination of these factors][col. 3, lines 11 – 67, col. 4, lines 1 – 47, lines 58 – 67, col. 5, lines 1 – 40, fig. 1].

10. As to claims 7, and 11, Shamir discloses counting of a certain numbers of instructions which inherently teaches a counter for measuring time interval between two instances too [col. 3, lines 23 – 25].

11. As to claims 8, and 12, Shamir discloses a chip and its memory that is configured to store parameters [col. 3, lines32 – 34, col. 1, lines 46 – 59, col. 2, lines 10 - 25] therefore it can configured to store any other time information too.

12. As to claims 9, and 13, Shamir discloses switchover logic which is triggered by a voltage of the discharging capacitor falling below predetermined threshold or by counting number of instructions which inherently measures time interval, or by combination of these factors therefore he teaches a time dependent upon a random variable too [col. 3, lines 22 – 29].

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 1 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shamir, US Patent 6,507,913 as applied to claim 1, and further in view of Doittau et al. [hereinafter as Doittau], US Patent 3,790,890 [cited in previous office action].

15. As to claim 1, Shamir teaches a data carrier [10, smart card] for communication of communication data with a base station [card reader], comprising: processing means [1, smart card chip] for the processing of communicated communication data [processing of communicated data is inherent to smart card chip], and voltage supply means [3,4 capacitors] which are arranged to receive an external supply voltage [2, external power supply] applied to the data carrier [10] during a charging time interval until a turn-on instant and which are adapted to supply an internal supply voltage to the processing means [1], decoupled [detached] from the external supply voltage [2] during consumption time interval starting at the turn-on instant [detachment during security critical computations] , the processing means being adapted to interrupt the processing from an interruption instant, when the internal supply voltage decreases below threshold voltage until the turn-on instant [switchover logic is triggered by a voltage of the discharging capacitor falling below predetermined threshold or by counting number of instructions which inherently measures time interval, or by combination of these factors][col. 3, lines 11 – 67, col. 4, lines 1 – 47, lines 58 – 67, col. 5, lines 1 – 40, fig. 1], characterized in that there are provided time measurement means [counter] which are adapted to measure [for

counting number of instructions which inherently teaches a counter for measuring processing time], and the voltage supply means [3, 4] are adapted to adapt the consumption time interval to the measured processing time interval [counting of a certain numbers of instructions which inherently teaches a counter for measuring processing time between two instructions col. 3, lines 23 – 25] [col. 3, lines 11 – 67, col. 4, lines 1 – 47, lines 58 – 67, col. 5, lines 1 – 40, fig. 1].

However, Shamir's time measurement means [counter] does not explicitly adapted to measure a processing time interval defined as the time interval from turn-on instant till interruption instant. In summary, he does not teach to measure time interval between the two instances.

Doittau teaches a device [2 1, measuring device] and method for measuring a time interval for charging a capacitor during a first time interval and discharging during a second time interval and possible different use of device to measure particular instances too [col. 1, lines 3 - 12, col. 5, lines 38 - 48, fig. 21].

It would have been an obvious to one of ordinary skill in art, having the teachings of Shamir and Doittau before him at the time of invention was made, to modify switchover logic [9] with power transistors [8] for power coupling and decoupling of external power supply [2] to the smart chip [1] disclosed by Shamir [col. 3, lines 11 – 67, col. 4, lines 1 – 67, col. 5, lines 1 – 32] to include and Doittau's device for measuring time interval for particular instances as both are related to control charging and discharging of capacitor and Doittau's teaching of measuring time interval provide a discharge curve which will enable the transition to give voltage threshold across capacitor and ratio between the charge and discharge can be controller with resistors [col. 1, lines 53 – 64].

16. As to claims 2 - 4, Doittau discloses that the voltage supply means adapted to reduce, prolong consumption time interval stepwise [an arrangement and use of resistors fig. 21 to accomplish the different value for ratio between charge and discharge times of capacitor] when consumption time interval (t2) is longer than the processing time interval (t1) [col. 2, lines 35 - 67, col. 3, lines 1 - 60, fig. 2 – 41].

17. As to claim 5, Doittau discloses a memory means (30, storage device) adapted to store power information [voltage amplitude] [col. 5, lines 17 – 491].

Conclusion

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
October 5, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
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